REMARKS

The Examiner is thanked for the careful review of the application as set out in the outstanding office action. Reconsideration of the application is respectfully requested.

Claims 4 and 5 have been amended to correct minor informalities.

Claims 1-13 stand rejected under 35 USC 102(b) as being anticipated by US 5,926,123 ("Ostrow"). The rejection is respectfully traversed on the grounds that a prima facie case of anticipation has not been established, and the applied reference does not describe each element of the claimed invention.

Claim 1 is drawn to a calibration method for optimizing the transfer function of analog-to-digital converter (ADC) employing a cascade of n stages to form a composite n-bit ADC transfer function, the ADC having an analog input and an n-bit digital output, each stage having an analog input, the method comprising:

applying a signal having a symmetric or uniform probability density property to the ADC analog input;

determining at least one error value for each stage resulting from application of said signal;

using the at least one error value for each stage to compensate each of said n stages during ADC operation.

Ostrow does not describe each limitation of Claim 1. For example, Ostrow does not disclose "applying a signal having a symmetric or uniform probability density property to the ADC analog input." Ostrow describes using a pseudo-random signal applied to a digital-to-analog converter 17, not to the ADC analog input. Thus, the Ostrow reference teaches a different calibration technique, and does not disclose all limitations of Claim 1. The rejection of Claim 1 and the claims depending therefrom should be withdrawn.

Claim 9 is drawn to an analog-to-digital converter (ADC), comprising:

a cascade of N-stages, wherein a first stage determines the most significant or coarse bit(s) for the ADC, and a last stage determines the least significant or finest resolution bit(s) for the ADC, the cascade of N-stages forming a composite n-bit ADC transfer function;

an ADC analog input port;

an ADC digital output port;

the first stage having a stage analog input connected to the ADC analog input port, and producing a first stage digital output and a first stage digital output;

a calibration circuit for optimizing the ADC transfer function in response to application to the ADC of a calibration signal having a symmetric or uniform probability density property to the ADC analog input, the calibration circuit for determining at least one error value for each stage resulting from application of said signal;

an error compensation circuit coupled to the calibration circuit for compensating each stage in response to said at least one error value for each stage.

Ostrow does not disclose each element of Claim 9, including for example "a calibration circuit for optimizing the ADC transfer function in response to application to the ADC of a calibration signal having a symmetric or uniform probability density property to the ADC analog input." Thus, the rejection of Claim 9, as well as the rejection of the claims depending therefrom, should be withdrawn.

Claim 13 is drawn to a calibration method for optimizing the transfer function of analog-to-digital converter (ADC) employing a cascade of n stages to form a composite n-bit ADC transfer function, the n stages including a first stage which determines the most significant or coarse bit(s), and a last stage which determines the least significant or finest resolution bit(s), the ADC having an analog input and an n-bit digital output, each stage having an analog input, the method comprising:

applying a signal having a symmetric or uniform probability density property to the ADC analog input;

determining at least one error value for each stage resulting from application of said signal, by examining statistics of bit transitions at each stage to compute bit transition probability density functions for both individual stage outputs and for logical combinations of the stage outputs to determine deviation from a desired transfer function related to both gain and offset errors within and between the stages;

using the at least one error value for each stage to compensate each of said n stages during ADC operation.

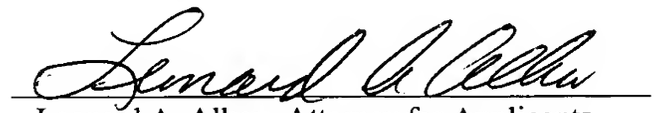
Ostrow does not disclose each element of the claimed invention, including, for example, "applying a signal having a symmetric or uniform probability density property to the ADC analog input." The rejection of Claim 13 should be withdrawn.

CONCLUSION

The outstanding rejection under Section 102(b) has been addressed, and the application is in condition for allowance. Such favorable reconsideration is solicited.

Respectfully submitted,

Registration No. 30,021



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

4. (Amended) The method of Claim 3, wherein said examining statistics of bit transitions includes:

computing bit transition probability density functions [are computed] for each stage output.

5. (Amended) The method of Claim 4, wherein said examining statistics of bit transitions includes:

computing the bit transition probability density functions for individual bits of each stage output and for logical combinations of said individual bits of each stage output to determine deviation from a desired ideal transfer function related to both gain and offset errors within and between the stages.